REMARKS

This paper responds to the Office Action mailed on January 26, 2006, and the references cited therewith.

No claims are amended or canceled; as a result, claims 1-58 are pending in this application.

Objection to the Specification

The specification has been amended to correct the typographical error. Applicant respectfully requests withdrawal of the objection.

§103 Rejection of the Claims

Claims 1-9, 16-22, 29-37 and 44-52 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ekstedt et al. (U.S. 5,206,582) in view of Chen et al. (U.S. 5,726,920).

Ekstedt describes a control system for automated parametric test equipment, including the ability to define and execute test sequences on such equipment. Ekstedt further teaches, as in the cited Figure 9's element 76, sequential control of both semiconductor test equipment such as a wafer loader, and parametric test equipment such as a prober.

Chen describes in the cited portion (col. 5, ln. 49-55) and in the accompanying Figure 1A a wafer test system in which a wafer electrical test (WET) in which one or a few basic elements such as transistors, resistors, or capacitors are tested for basic electrical functionality after a wafer is removed from a transport cassette 103 but before the wafer is inserted into a final wafer sort test station 110..

In contrast, the pending claims describe an automated semiconductor parametric test system having a control module operable to control concurrent operation of semiconductor test equipment and of parametric test instrumentation. Ekstedt explicitly describes sequential control of semiconductor test equipment and parametric test equipment, and so fails to anticipate concurrent control as is claimed. Chen also fails to disclose any example in which semiconductor test equipment and parametric test equipment are concurrently controlled. Chen's description at col. 5, ln. 53-55 that wafer electrical testing (WET) is understood to already have

occurred along the movement path 104 prior to wafer insertion in the final wafer sort test station does not imply that the test was performed while the robot is actually moving the wafer, but merely states that the WET test takes place after the wafer is removed from a cassette but before it is loaded in the final wafer test station for parametric testing.

More specifically, basic elements tested in the wafer electrical test are described as probed elements (see col. 2, ln. 7-8), and the prober of Chen is explicitly defined as including alignment system 112 and chuck 114, indicating that the probed wafer is in the chuck and uses the alignment system for probing as part of the wafer electrical test. Further, the test station 110 is defined as including both a generic test head system 118-119 used to probe generic elements, such as individual components probed in the wafer electrical test (WET test). The test station 110 also includes other features not needed for the WET test such as product specific test-head system components 115-117, suggesting that these separate features are used as part of the test station only after the wafer electrical test.

The wafer electrical test is described in detail in the background's col. 1, ln. 66 – col. 2, ln 29, in which a short electrical test of basic electrical components such as individual capacitors, resistors, and transistors takes from one to ten minutes, and is repeated in the event of a negative test result to ensure the accuracy of the test, suggesting the test takes significantly longer than the amount of time needed to lift a wafer from a cassette and load it into a final wafer test station. Nothing suggests that the wafer is in the robotic arm or that the robotic arm remains in controlled motion or is moving while the wafer electrical test takes place, and the sections of Chen discussed above indicate that the wafer is in fact loaded into a prober including at least a chuck and alignment system for wafer electrical testing.. No robotic moving probe set operable to track a moving wafer with the precision necessary to contact and track a microscopic electrical contact pad on a wafer is described in Chen or otherwise known in the art, further indicating that "already occurred along the movement path 104 prior to insertion into the FWS test station" does not mean that a wafer is probed while being held in a robotic arm in motion.

One skilled in the art would conclude that an interpretation that wafer electrical testing occurs while the robot arm is in motion is not possible using current technology, is not enabled by the cited Chen reference, is contrary to what the Chen reference teaches regarding probing

including a chuck and alignment system, and is not what is meant by the cited language in lines 49-55 of column 5.

Because neither of the cited references teaches concurrent control of operation of semiconductor test equipment and of operation of parametric test instrumentation, the pending claims are distinct from the cited references. Reexamination and allowance of these pending claims is therefore respectfully requested.

Claims 10-15, 23-28, 38-43 and 53-58 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ekstedt et al. in view of Chen et al. as applied to claims 1, 16, 29 and 44 above, and further in view o f Gloudeman et al. (U.S. 6,119,125).

Because these claims depend from claims shown above to be allowable in view of the cited references, these claims are further believed to be allowable as dependent on allowable base claims. Further, none of these references shows concurrent control of operation of semiconductor test equipment and of operation of parametric test instrumentation, and so these claims are allowable over the references cited here.

Reexamination and allowance of these claims is therefore respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9581 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date Apr. 26 06

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 26 day of April, 2006.

KATE GANNON
Name

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Signature